Amendments to the Specification:

1) page 6, second paragraph, please replace this paragraph with the following amended text:

Fig. 1 shows a cross section of a semiconductor surface on the surface of which a contact pad has been created, the semiconductor surface is covered with a patterned layer of passivation,

Fig. 2 shows the cross section of Fig. 1 after a patterned layer of dielectric and a layer of metal have been created on the semiconductor surface,

Fig. 3 shows a cross section of Fig. 2 after a layer of interconnect metal and a layer of solder compound have been selectively deposited, and

Fig. 4 shows a cross section after ~~excessive~~ excess layers have been removed from the semiconductor surface and after the solder has been flowed, forming the interconnect bump.

2) page 6, last paragraph, page 7, first paragraph, please replace this paragraph with the following amended text:

Figs. 5 through 12 show the process of the invention, ~~s~~ as follows:

Fig. 5 shows a cross section of a semiconductor surface on the surface of which a contact pad has been created, the semiconductor surface is covered with a layer of passivation, a layer of UBM has been deposited.

3) page 8, first paragraph, please replace this paragraph with the following amended text:

Figs. 13 and 14 show a prior art ~~creation of a~~ solder bump, ~~for the purposes of~~ highlighting problems that are typically experienced in creating such a solder bump.

4) page 8, last paragraph, page 9, first paragraph, please replace this paragraph with the following amended text:

Fig. 1 shows an example of one of the conventional methods that can be used to create an interconnect bump.

A semiconductor surface 10 has been provided with a metal contact pad 14, the semiconductor surface 10 is protected with a layer 12 of passivation. An opening 11 has been created in the

layer 12 of passivation, the surface of the metal contact pad 14 is exposed through this opening 11.

Next, as shown in the cross section of Fig. 2, a dielectric layer 16 is deposited over the surface of the layer 12 of passivation. The layer 16 of dielectric is patterned and etched, creating an opening 13 in the layer 16 of dielectric that aligns with the metal pad 14 and that exposes the surface of the metal pad 14.

A layer of 18 of metal, also shown in the cross section of Fig. 2, typically created by applying Under Bump Metallurgy (UBM), is ~~created~~ deposited over the layer 16 of dielectric, this layer 18 of metal is in contact with the surface of the metal pad 14 inside opening 13. The layer 18 of metal that is above the metal pad 14 will, at a later point in the process, form a pedestal over which an interconnect bump will be formed.

This pedestal can ~~be~~ further be extended in height by the deposition and patterning of one or more additional layers (underlying the pedestal 18 shown in the cross section of Fig. 2) that may contain a photoresist or a dielectric material. These additional layers have not been shown in Fig. 2 but essentially have the shape of layer 16 and can be removed during

one of the final processing steps that are applied for the formation of the interconnect bump.

5) page 14, first and second paragraph, please replace this paragraph with the following amended text:

In-situ sputter clean has been performed of the exposed surface of the contact pad 14. A seed layer (not shown in Fig. 5) has been blanket deposited over the surface of the layer 12 of passivation, including the exposed surface of the contact pad 14, a film 18 of Under Ball Metallurgy has been blanket deposited over the seed layer.

~~Layer 10 is the surface of a semiconductor layer, a contact pad 14 has been created on surface 10. Surface 10 will typically be the surface of a semiconductor substrate, the surface of an interconnect substrate and the like. A contact pad 14 has been created on surface 10, electrical contact must be established with contact pad 14 by means of an overlying solder bump. Contact pad 14 serves as interface between the solder bump and electrical interconnects that are provided in the surface of layer 10.~~

~~Contact pad 14 can include a contact pad that is formed on a surface other than the surface of a substrate, such as the~~

~~surface of a printed circuit boards, flex circuits or a metallized or glass substrate or semiconductor device mounting support.~~

6) page 14, last paragraph, page 15, first paragraph, please remove this paragraph:

~~A layer 12 of passivation that may, for instance, contain Plasma Enhanced silicon nitride (PE Si_3N_4), is deposited over the surface of layer 10 and of contact pad 14. Layer 12 of passivation material may also have been created using successive and overlying depositions of layers of passivation material. The passivation layer 12 deposited over the surface of the semiconductor surface comprises a plurality of passivation layers. The plurality of passivation layers may be selected from such materials as PE Si_3N_4, SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.~~

7) page 18, second paragraph, please replace this paragraph with the following amended text:

Layer 12 of passivation ~~layer~~ material, deposited over the ~~surface of said~~ semiconductor surface 10, can also comprise a

plurality of passivation layers, ~~this to provide~~ providing improved protection to underlying surfaces. This plurality of passivation layers can for instance be selected from a group comprising PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide and titanium nitride.

8) page 18, fourth paragraph, please replace this paragraph with the following amended text:

For ~~the~~ an in-situ sputter clean of the exposed surface of contact pad 14, a sputter ion-milling tool can be used, ~~using~~ applying Ar mixed with H_2 as a cleaning agent (sputter source).

9) page 20, fourth paragraph, please replace this paragraph with the following amended text:

Fig. 7 shows a cross section during the exposure of the layer 31 of photoresist. Exposure mask 32 is used for this ~~purposed of~~ exposure, on the surface of quartz substrate 34 of mask 32 are two concentric patterns 33 (a first pattern) and 36 (a second pattern) of opaque material, making mask 32 a grey-tone mask.

10) page 22, second paragraph, please replace this paragraph with the following amended text:

The reasons that the T-shape of the created layer 41 is of benefit can be explained as follows~~: if~~. If the surface area of the patterned layer of UBM is larger than the surface area of the contact pad, ~~the die crack will~~ die cracks 43, shown in the cross section of Fig. 13, are likely to occur between the solder bump 42 and the underlying layer 18 of UBM. By limiting the size of the surface area of the layer of UBM to the same size as the size the surface area of the contact pad, cracking ~~is~~ can be prevented ~~as has been shown in the cross section of Fig. 14~~. However, limiting the ~~size~~ the surface area of the patterned layer of UBM layer underlying the solder bump leads to limiting the size of the solder bump~~, see Fig. 15~~. By therefore creating a T-shaped solder form, more solder can be deposited, thereby creating ~~s~~ a larger solder bump without creating a layer of UBM as the footprint of the solder bump.

11) page 1, the title of the invention, please replace the title ~~NOVEL METHOD TO IMPROVE BUMP RELIABILITY FOR FLIP CHIP DEVICE~~ with the new title METHOD FOR IMPROVING BUMP RELIABILITY FOR FLIP CHIP DEVICES

Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

1. (currently amended) A method ~~to improve~~ to create a solder bump ~~reliability~~ for interconnection of flip chip devices, comprising the steps of:

providing a substrate, at least one [[a]] contact pad having been provided over ~~the surface of~~ said substrate, a layer of passivation having been deposited over ~~the surface of~~ said substrate, said layer of passivation having been patterned ~~and etched~~, exposing ~~the surface of~~ said at least one contact pad, a layer of ~~Under Ball Metal~~ Under-Bump-Metallurgy (UBM) having been deposited over ~~the surface of~~ said layer of passivation including the exposed ~~surface of~~ said at least one contact pad;

creating at least one T-shaped layer of solder compound over ~~the surface of~~ said layer of UBM in at least one opening created in a layer of patterning material, said at least one T-shaped layer of solder compound being aligned with said at least one contact pad having been provided over ~~the surface of~~ said substrate, said creating at least one T-shaped layer of solder compound over said layer of UBM comprising:

(i) depositing said layer of patterning material over said layer of UBM; and

(ii) patterning and developing said layer of patterning material using a grey-tone mask;

removing said layer of patterning material, leaving in place said at least one T-shaped layer of solder compound, exposing ~~the surface of~~ said ~~patterned layers~~ layer of UBM;

etching said exposed layer of UBM using said at least one T-shaped layer of solder compound as a mask; and

reflowing ~~the surface of~~ said solder compound, creating said solder bump.

2. (original) The method of claim 1, said layer of patterning material comprising photoresist.

3. (original) The method of claim 1, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

4. (original) The method of claim 1, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

5. (currently amended) The method of claim 1, said passivation layer deposited over ~~the surface of~~ said semiconductor surface comprising a plurality of passivation layers.

6. (original) The method of claim 5, at least one of said plurality of passivation layers being selected from the group consisting of PE Si_3N_4 and SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

7. (currently amended) The method of claim 1, said at least one contact pad on said semiconductor ~~surface~~ substrate being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

8. (currently amended) The method of claim 1, said at least one contact pad on said semiconductor substrate further being expanded to include a contact pad that is formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

9. (currently amended) The method of claim 1 with an additional step of applying a solder flux to ~~the surface of~~ said solder compound, said additional step ~~to be~~ being performed immediately prior to said reflowing ~~the surface of~~ said solder compound.

10. (currently amended) The method of claim 1, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad ~~by a measurable amount~~, simultaneously creating conductive interconnect lines on ~~the surface of~~ said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

Claim 11. (cancelled).

12. (currently amended) The method of claim [[11]] 1 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material, said at least one pattern of two concentric patterns comprising a first pattern and a second pattern;

[[a]] said first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern, said first pattern having a first thickness;

[[a]] said second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on ~~the surface of~~ said substrate, said second pattern having a second thickness; and

said first thickness being larger than said second thickness ~~first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount~~.

13. (currently amended) The method of claim [[11]] 1, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

14. (currently amended) The method of claim 13, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

15. (currently amended) A method ~~to improve~~ to create a solder bump ~~reliability~~ for interconnection of flip chip devices, comprising the steps of:

providing a substrate, active semiconductor devices having been created in or on ~~the surface of~~ said substrate;

creating at least one [[a]] contact pad over ~~the surface of~~ said substrate;

depositing a layer of passivation ~~having~~ over ~~the surface of~~ said substrate, including ~~the surface of~~ said at least one contact pad;

patterning ~~and etching~~ said layer of passivation, exposing ~~the surface of~~ said at least one contact pad;

depositing a layer of ~~Under Ball Metal~~ Under-Bump-Metallurgy (UBM) over ~~the surface of~~ said layer of passivation, including ~~the exposed surface of~~ said at least one contact pad;

depositing a layer of exposure sensitive material over ~~the surface of~~ said layer of UBM;

patterning ~~and etching~~ said layer of exposure sensitive material, creating at least one opening having a T-shaped cross section through said exposure sensitive material, said at least one opening being aligned with said at least one contact pad created over ~~the surface of~~ said substrate, said creating at

least one opening having a T-shaped cross section through said exposure sensitive material comprising:

(i) depositing said layer of exposure sensitive material over said layer of UBM; and

(ii) patterning and developing said layer of exposure sensitive material using a grey-tone mask;

filling said at least one opening created through said exposure sensitive material with a solder compound;

removing said exposure sensitive material from ~~the surface of~~ said layer of UBM, leaving in place at least one T-shaped layer of solder compound, exposing ~~the surface of~~ said layer of UBM;

etching said layer of UBM, using said at least one T-shaped layer of solder compound as a mask; and

reflowing said at least one T-shaped layer of solder compound.

16. (original) The method of claim 15, said layer of exposure sensitive material comprising photoresist.

17. (original) The method of claim 15, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

18. (original) The method of claim 15, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

19. (currently amended) The method of claim 15, said passivation layer deposited over ~~the surface of~~ said semiconductor surface comprising a plurality of passivation layers.

20. (original) The method of claim 19, at least one of said plurality of passivation layers being selected from the group consisting of PE Si_3N_4 and SiO_2 and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

21. (currently amended) The method of claim 15, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

22. (currently amended) The method of claim 15, said at least one contact pad on said semiconductor substrate further being expanded to include a at least one contact pad that is formed on

a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

23. (currently amended) The method of claim 15, with an additional step of applying a solder flux to ~~the surface of~~ said solder compound, said additional step ~~to be~~ being performed immediately prior to said reflowing ~~the surface of~~ said solder compound.

24. (currently amended) The method of claim 15, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad by a measurable amount, simultaneously creating conductive interconnect lines on ~~the surface of~~ said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

Claim 25: (cancelled).

26. (currently amended) The method of claim [[25]] 15 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material, said at least one pattern of two concentric patterns comprising a first pattern and a second pattern;

[[a]] said first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern, said first pattern having a first thickness;

[[a]] said second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on ~~the surface of~~ said substrate, said second pattern having a second thickness; and

said first thickness being larger than said second thickness ~~first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount~~.

27. (currently amended) The method of claim [[25]] 15, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

28. (currently amended) The method of claim 27, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material ~~and said exposed surface of said layer of UBM~~.

Please add the following new claims:

29. A solder bump for interconnection of flip chip devices, comprising:

a substrate, active semiconductor devices having been created in or over said substrate;

at least one contact pad created over said substrate;

a patterned layer of passivation created over said substrate, said patterned layer of passivation exposing said at least one contact pad;

a patterned layer of Under-Bump-Metallurgy (UBM) created over said layer of passivation, including said at least one contact pad, a surface area of the patterned layer of UBM being limited to a size no larger than a size of a surface area of the at least one contact pad; and

at least one layer of reflown solder compound overlying said patterned layer of UBM.

30. The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

31. The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

32. The solder bump of claim 29, said patterned layer of passivation comprising a plurality of passivation layers.

33. The solder bump of claim 32, wherein at least one of said plurality of passivation layers is PE Si_3N_4, SiO_2, a photosensitive polyimide, phosphorous doped silicon dioxide or titanium nitride.

34. The solder bump of claim 29, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

35. The solder bump of claim 29, said at least one contact pad on said semiconductor substrate further comprising a contact pad formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

36. The solder bump of claim 29, with a seed layer having been deposited over said patterned layer of passivation.